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Bidirectional converter for high-efficiency fuel cell powertrain

Abbas A. Fardoun [a,*], Esam H. Ismail [b], Ahmad J. Sabzali [b], Mustafa A. Al-Saffar [b]

[a] Electrical Engineering Department, University of United Arab Emirates, P.O. Box 15551, Al-Ain, United Arab Emirates
[b] Electrical Engineering Department, College of Technological Studies, P.O. Box 35007, Al-Shaab 36051, Kuwait

HIGHLIGHTS

- A wide conversion ratio step-up/down bidirectional dc–dc converter is proposed.
- Single control signal in charging/discharging modes with low switch voltage stress.
- Extending battery and fuel cell service life due to the low current ripple.
- Synchronized switching of the converter can further improve the system efficiency.
- Voltage stresses on all semiconductors are *g* reduced.

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ABSTRACT

In this paper, a new wide conversion ratio step-up and step-down converter is presented. The proposed converter is derived from the conventional Single Ended Primary Inductor Converter (SEPIC) topology and it is integrated with a capacitor–diode voltage multiplier, which offers a simple structure, reduced electromagnetic interference (EMI), and reduced semiconductors' voltage stresses. Other advantages include: continuous input and output current, extended step-up and step-down voltage conversion ratio without extreme low or high duty-cycle, simple control circuitry, and near-zero input and output ripple currents compared to other converter topologies. The low charging/discharging current ripple and wide gain features result in a longer life-span and lower cost of the energy storage battery system. In addition, the "near-zero" ripple capability improves the fuel cell durability. Theoretical analysis results obtained with the proposed structure are compared with other bi-direction converter topologies. Simulation and experimental results are presented to verify the performance of the proposed bi-directional converter.

1. Introduction

Alternative energy systems such as fuel cell (FC) and photovoltaic (PV) are open loop systems where the output power always changes as a function of the operating point (load and operating temperature) [1]. The electrochemical nature of the fuel cell dictates several constraints and/or requirements on the power flow subsystems. For instance, the slow time response of a fuel system calls for back-up power at starting conditions. Also, the current ripple effect on the quality of the fuel cell requires minimization of current ripple [2–4].

In the literature, there have been several power flow configurations to address these issues [5–12]. The configuration in Fig. 1 is a common configuration. The DC/DC converter of Fig. 1 is added as a power interface to regulate the output voltage and to cancel out the low frequency harmonics (100 Hz/120 Hz) injected by the AC load. Low frequency ripple cancellation ripple techniques based on feed forward and active ripple compensation techniques have been introduced in Refs. [13,14]. However, it has been reported that even though high frequency ripple component may not affect the fuel cell stack performance, nevertheless, it affects the characteristics of the fuel cell resulting in lower durability of the system [15,16]. Hence, the high frequency ripple generated by the converter or bidirectional converter would affect the durability of the fuel cell.

The bidirectional DC–DC converter is required to process power from batteries to the load during transient/start-up and overload conditions. The bidirectional converter has the following requirements: high gain to utilize lower cost low voltage batteries and low current ripple on the battery side to minimize the thermal stresses on the battery [17,18]. It should be noted that a series of batteries can eliminate the requirement of high input/output voltage ratio. However, slight mismatches in operating point can cause battery system imbalance resulting in higher stress; hence,

* Corresponding author. Tel.: +971 503385677; fax: +971 3713 4970.
E-mail addresses: abbasfardoun@gmail.com, afardoun@uaeu.ac.ae (A.A. Fardoun), eismail@ieee.org (E.H. Ismail), asebzali@ieee.org (A.J. Sabzali), malsaffar@ieee.org (M.A. Al-Saffar).

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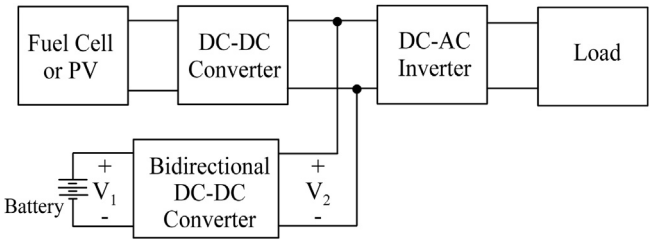

Fig. 1. Typical renewable energy system power flow diagram.

lower system reliability and shorter battery life span. A low power processing train for fuel cell application has been proposed in Ref. [9] and shown in Fig. 2. This configuration improves the system efficiency due to its reduced power processing stages. However, this configuration is more susceptible to the switching frequency ripple component of the bidirectional converter because both are connected to the same bus. Hence, a low ripple topology on the bus voltage side as well as the bus voltage side is extremely desired.

Bidirectional converter topologies have been developed based on isolated and non-isolated topologies depending on application requirement. Transformer isolated topologies require high number of switching devices [19–25]. In addition, soft switching is typically implemented to enhance the efficiency by reducing switching losses [26–29]. Therefore, the cost of the system increases and the control scheme becomes more complicated. This paper focuses on non-isolated topologies.

Non-isolated topologies are mainly based on the buck-boost configuration [30–32]. Buck-boost topology is fairly simple and easy to control; however, for low ripple requirement on the battery side, this topology requires a relatively high inductor at the battery side to smoothen the current leading to a slower dynamic response and has high switching losses. Soft switching has been proposed in Refs. [33–36]. However, these topologies still have pulsating current on the bus voltage side which results in high ripple and high electro-magnetic emissions. On the other hand, for high gain requirements, the converter requires an extreme duty-cycle operation resulting in serious reverse-recovery problems and increases the rating of the output diode. Consequently, the conversion efficiency is degraded, and the electromagnetic interference (EMI) problem is severe under this situation. To extend the gain range, interesting magnetic coupling techniques have been proposed in Refs. [37,38]. However, both converters have complex gating circuitry and pulsating bus voltage. A new high efficiency and fairly simple gating circuitry is presented in Ref. [39]. However, this topology still has pulsating bus voltage.

In this paper, a new DC–DC converter bidirectional topology is proposed. The proposed DC–DC converter topology has the following advantages: a) High gain ratio, b) Continuous input and output current; hence reduced ripple current in the output capacitors resulting in near-zero charging/discharging ripple, c) Galvanic isolation capability, d) Simple control circuitry, since it

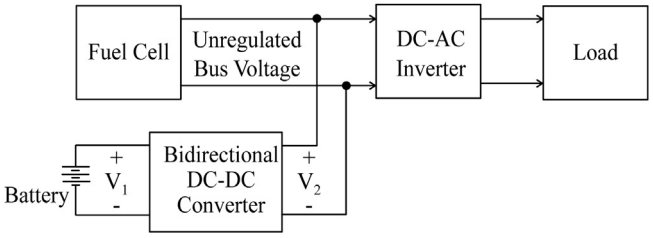

Fig. 2. High efficiency power flow configuration.

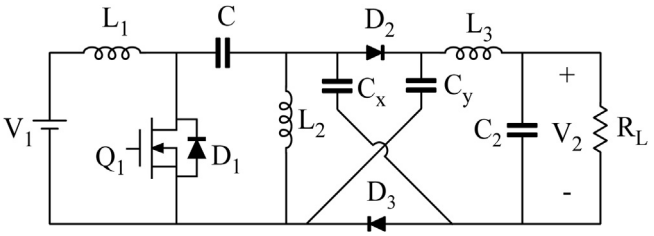

Fig. 3. Modified SEPIC converter [40].

requires only one control signal for both charging and discharging power flow, e) The individual inductors can be coupled on the same core; hence, the weight and size of the converter are reduced, and f) The converter switches can operate as synchronous switches, which can further improve the overall system efficiency.

2. The proposed bi-directional DC–DC converter

Fig. 3 shows the high gain SEPIC converter with continuous input/output current and voltage-doublers characteristics [40]. By replacing the two diodes (D_2 and D_3) with independently controlled active switches such as power MOSFETs, the circuit can operate as a bidirectional converter as shown in Fig. 4(a). Fig. 4(b) illustrates the isolated version of the converter in Fig. 4(a). The additional components in the proposed converter allow it to

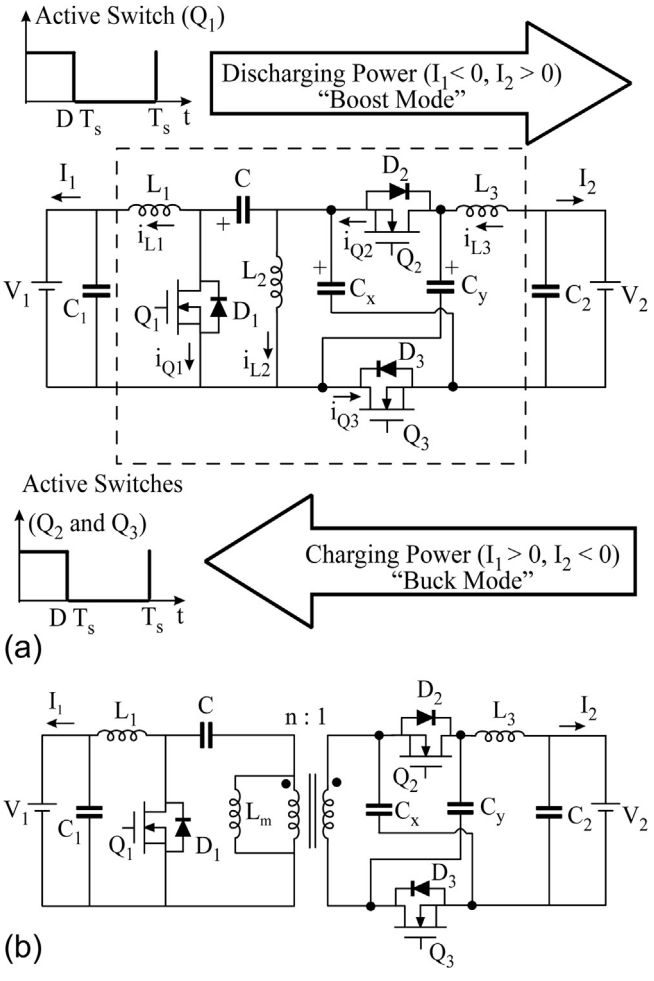

Fig. 4. Proposed SEPIC derived bidirectional converter. (a) Non-isolated topology. (b) Isolated topology.

operate differently from the original converter of Fig. 3. The proposed converter of Fig. 4 operates in two modes: (i) buck mode (step-down mode), charging the battery V_1; and (ii) boost mode (step-up mode), discharging the battery V_1. The gating signals of the active switches for each mode are illustrated in Fig. 4(a). During the boost mode operation (discharging power), switch Q_1 is switched on/off while switches Q_2 and Q_3 act as passive switches. In other words, the body diodes, D_2 and D_3, of Q_2 and Q_3; respectively, are utilized in the discharging power direction. In the charging mode (or step-down) operation, switches Q_2 and Q_3 operate as active switches, while the body diode D_1 of switch Q_1 is utilized.

2.1. Principle of operation and analysis (Buck mode)

To simplify the analysis; it is assumed that the converter of Fig. 4(a) is operating in a steady-state and in the charging power direction (Buck mode) with the following assumptions over one switching cycle (T_s): a) Input voltage (V_2) is pure dc. b) All components are ideal. c) All inductors and capacitors are sized to have a relatively small current and voltage ripple at the switching frequency f_s. d) Capacitors C_x and C_y have the same capacitance rating. Based on these assumptions, the circuit of Fig. 4(a) is analyzed next in continuous conduction mode (CCM).

When the converter operates in CCM, the circuit operation over one switching cycle (T_s) can be divided into two stages as shown in Fig. 5(a) and (b) and described as follows:

Stage 1 [$0 < t < D\,T_s$], Fig. 5(a): At the beginning of this stage, the power switches Q_2 and Q_3 are turned-on simultaneously. As a result, the two capacitors (C_x and C_y) appear in parallel configuration. Hence, they are charged equally by the inductor current i_{L3}. Inductor L_2 is being charged by the input voltage, and the energy stored in capacitor C is charging the load through L_1.

Stage 2 [$D\,T_s < t < T_s$], Fig. 5(b): at the begging of this stage, the switches Q_2 and Q_3 are turned-off. Thus, the body diode of switch Q_1 is turned on, allowing capacitor C to be charged by the energy stored in L_2. In this stage, the two capacitors C_x and C_y are effectively in series; hence, they are being discharged across C equally.

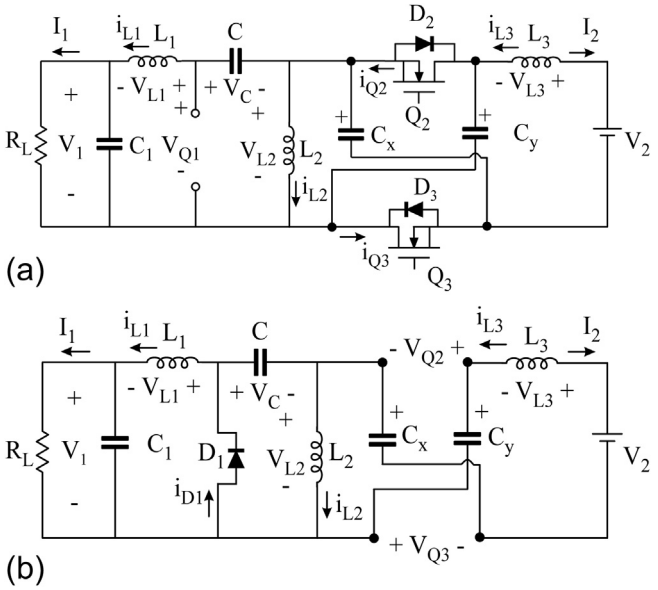

Fig. 5. Topological stages for the converter of Fig. 4(a) in charging power direction. (a) Stage 1. (b) Stage 2.

Based on the previous analysis, the voltages across L_1, L_2, and L_3 during the on-time of switches Q_2 and Q_3 are given by

$$\left.\begin{aligned} V_{L1} &= V_C + V_{Cx} - V_1 \\ V_{L2} &= V_{Cx} \\ V_{L3} &= V_2 - V_{Cx} \end{aligned}\right\} \quad t \in [0, DT_s] \tag{1}$$

and during Q_2 and Q_3 off-time are given by

$$\left.\begin{aligned} V_{L1} &= -V_1 \\ V_{L2} &= -V_C \\ V_{L3} &= V_2 - V_C - 2V_{Cx} \end{aligned}\right\} \quad t \in [DT_s, T_s] \tag{2}$$

According to the volt-second balance principle, the volt–second relationship of inductors L_1, L_2, and L_3 can be expressed as

$$D(V_C + V_{Cx} - V_1) - D'V_1 = 0 \tag{3}$$

$$DV_{Cx} - D'V_C = 0 \tag{4}$$

$$D(V_2 - V_{Cx}) + D'(V_2 - V_C - 2V_{Cx}) = 0 \tag{5}$$

respectively, where D is the duty-cycle of the switches Q_2 and Q_3 and $D' = 1 - D$ is the normalized switch-off time. The input-to-output voltage transfer ratio M_C in the charging direction of the proposed converter can be determined from (3)–(5), as

$$M_C = \frac{V_1}{V_2} = \frac{D}{2D'} \tag{6}$$

Theoretical CCM waveforms of the proposed converter during buck mode are shown in Fig. 6(a).

2.2. Principle of operation and analysis (boost mode)

Fig. 7 shows the topological stages for the converter of Fig. 4(a) in discharging power direction (boost mode). Similar to the buck mode, when the converter operates in CCM, the circuit operation over one switching cycle (T_s) can be divided into two stages as shown in Fig. 7(a) and (b) and described as follows:

Stage 1 [$D\,T_s < t < T_s$], Fig. 7(a): At the instant DT_s, power switch Q_1 is turned-on, the body diodes of switch Q_2 and Q_3 (i.e. D_2 and D_3) are turned-off by the negative voltage ($V_C + V_{Cx}$) across them. In this stage, the current through both the capacitors C_x and C_y are the same, and it is equal to the inductor L_3 current. Thus, in this stage, both capacitors C_x and C_y are effectively in series charging the load. At the end of this interval, the switch Q_1 is turned-off initiating the next subinterval.

Stage 2 [$0 < t < D\,T_s$], Fig. 7(b): At the beginning of this interval, switch Q_1 is turned-off, the body diodes D_2 and D_3 are turned-on simultaneously providing a path for the input and output inductor currents. In this stage, the two capacitors C_x and C_y are effectively in parallel; hence, they are being charged equally.

Based on the previous analysis, the voltages across L_1, L_2, and L_3 during the switch Q_1 on-time are given by

$$\left.\begin{aligned} V_{L1} &= V_1 \\ V_{L2} &= V_C \\ V_{L3} &= 2V_{Cx} + V_C - V_2 \end{aligned}\right\} \quad t \in [DT_s, T_s] \tag{7}$$

and during Q_1 off-time are given by

$$\left.\begin{aligned} V_{L1} &= V_1 - V_C - V_{Cx} \\ V_{L2} &= -V_{Cx} \\ V_{L3} &= V_{Cx} - V_2 \end{aligned}\right\} \quad t \in [0, DT_s] \tag{8}$$

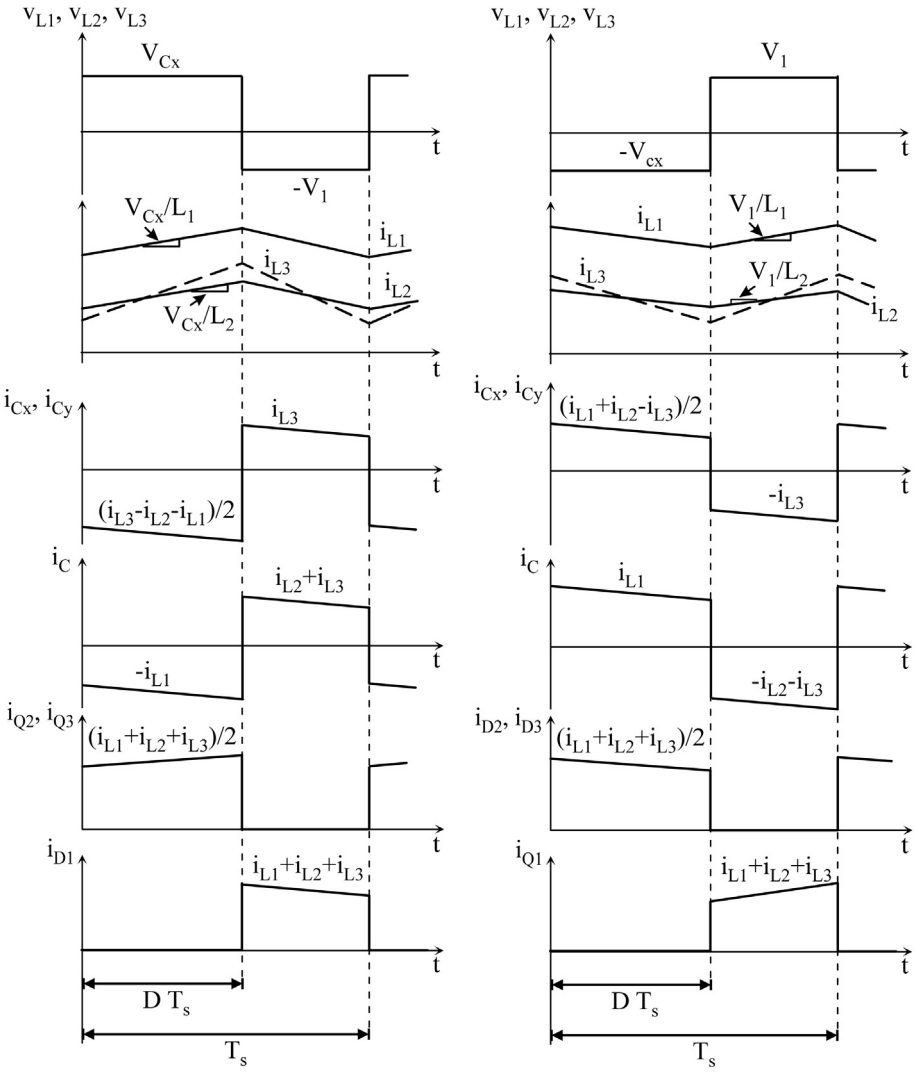

Fig. 6. Key waveforms for the proposed converter of Fig. 4(a).

According to the volt–second balance principle, the volt–second relationship of inductors L_1, L_2, and L_3 can be expressed as

$$D'V_1 + D(V_1 - V_C - V_{Cx}) = 0 \tag{9}$$

$$D'V_C - DV_{Cx} = 0 \tag{10}$$

$$D'(2V_{Cx} + V_C - V_2) + D(V_{Cx} - V_2) = 0 \tag{11}$$

Hence, from [9–11], the voltage gain M_D in the boost mode can be derived and is given by

$$M_D = \frac{V_2}{V_1} = \frac{2D'}{D} \tag{12}$$

The voltage gain in the boost mode [12] is the reciprocal of the voltage gain in the buck mode [6]. One can also show that the three inductors have identical ac voltage waveforms regardless the operation mode. Note that [7] and [8] are identical to [2] and [1], respectively, except that one is the negative of the other. This is because the voltage variables across the three inductors in Fig. 7 are assigned in opposite direction compared to Fig. 5. Theoretical CCM waveforms during boost mode are shown in Fig. 6(b). The operating principle in the Discontinuous Conduction Mode (DCM) for the boost mode is given next.

2.3. Discontinuous Conduction Mode (boost mode)

The DCM for the proposed SEPIC topology occurs when the current through diodes D_2 and D_3 drops to zero value before the end of the switch off-time. Thus, there are three operating stages in DCM. The first stage is similar to the first CCM stage. During the second stage, the diode currents (i_{D2} and i_{D3}) reach zero before the end of the switch Q_1 off-time. Hence, at the onset of DCM, a third topological stage appears where all the semiconductors are off. The three inductors behave as current sources, which keep currents constant. The capacitors C is being charged by the input current i_{L1} while the capacitors C_x and C_y are being charged by the output inductor current i_{L3}. The voltages across the three inductors are zero. The three inductors current waveforms and the diode current waveform DCM are shown in Fig. 8 for the case when $L_2 = L_3$. Referring to Fig. 8 and according to the volt–second balance on L_1, L_2, and L_3, the following relation is obtained

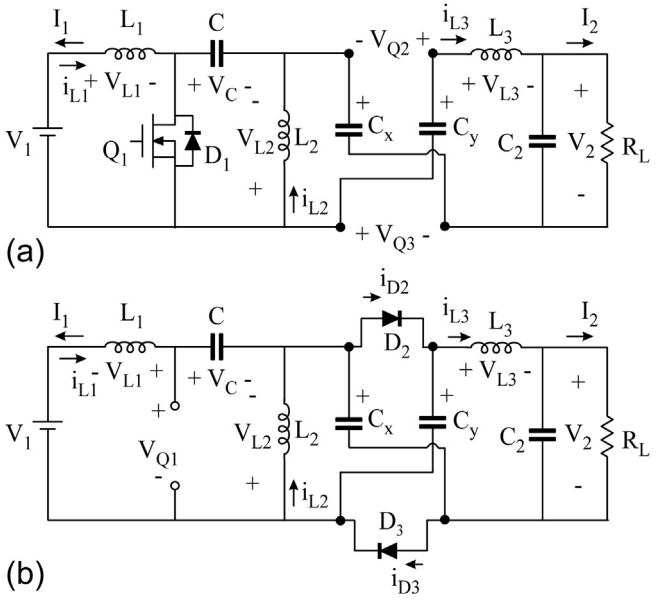

Fig. 7. Topological stages for the converter of Fig. 4(a) in discharging power direction. (a) Stage 1. (b) Stage 2.

$$d_2 = 2D'\frac{V_1}{V_2} \tag{13}$$

Furthermore, at steady-state, the average diode currents (i_{D2} and i_{D3}) over one switching period must equal the output current, i.e.,

$$I_2 = \bar{i}_{D2} = \frac{1}{2} \times d_2 \times I_{D2-pk} \tag{14}$$

where the peak diode current $I_{D2\text{-}pk}$ is given by,

$$I_{D2-pk} = \frac{V_1 D' T_S}{2L_e} \tag{15}$$

and

$$\frac{1}{L_e} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3} \tag{16}$$

Substituting [13] and [15] in [14], the voltage conversion ratio in DCM is obtained as

$$M_{D-DCM} = \frac{D'}{\sqrt{K_e}} \tag{17}$$

where the dimensionless parameter K_e is defined as

$$K_e = \frac{2L_e}{R_L T_s} \tag{18}$$

2.4. Boundaries between CCM and DCM

From the waveforms in Fig. 8, the DCM operation mode requires that

$$d_2 < D \tag{19}$$

Substituting [13] into [19] and using [12] and [17], the following condition for DCM is obtained,

$$K_e < K_{e-crit} = \frac{D^2}{4} = \frac{1}{(M_D + 2)^2} \tag{20}$$

For values of $K_e > K_{e-crit}$, the converter operates in CCM. Otherwise, the converter operates in DCM. The DCM analysis for the Buck mode can be obtained by following the same procedure outlined for the boost mode case.

2.5. Component stresses

Table 1 shows the normalized component voltage and current stresses of the proposed converter of Fig. 4(a). Voltages and currents are normalized with respect to V_2 and I_2, respectively. These equations are given for design purposes. The component stresses in Table 1 are valid for both charging and discharging mode provided that $M = V_2/V_1$. Referring to Table 1, it is clear that the switch Q_1 is subjected to a relatively higher rms current stress since it must supply current to three inductors. However, the low switch voltage stress enable the use of a lower voltage rated with low $R_{DS(ON)}$ which greatly reduces switch conduction losses.

2.6. Large-signal average model

The averaged model for the proposed converter of Fig. 4(a) when the three inductors L_1, L_2, and L_3 are in CCM is derived based on averaging passive and active switches waveforms during one switching cycle T_s.

Referring to Figs. 5(a) and 7(b), the average voltage across the switch Q_1 is given by

$$< v_{Q1} >_{Ts} = E_{Q1} = D(v_C + v_{Cx}) \tag{21}$$

and from Fig. 6 the average current through switches Q_2 and Q_3 can be determined by

$$< i_{Q2} >_{Ts} = < i_{Q3} >_{Ts} = G_{Q2} = G_{Q3} = \frac{D}{2}(i_{L1} + i_{L2} + i_{L3}) \tag{22}$$

Fig. 9 shows the complete averaged model for the proposed converter of Fig. 4(a). This model predicts both steady-state and transient responses of the converter. Moreover, the same model can be used in frequency domain analysis to obtain small-signal transfer function of the converters to aid in the controller design.

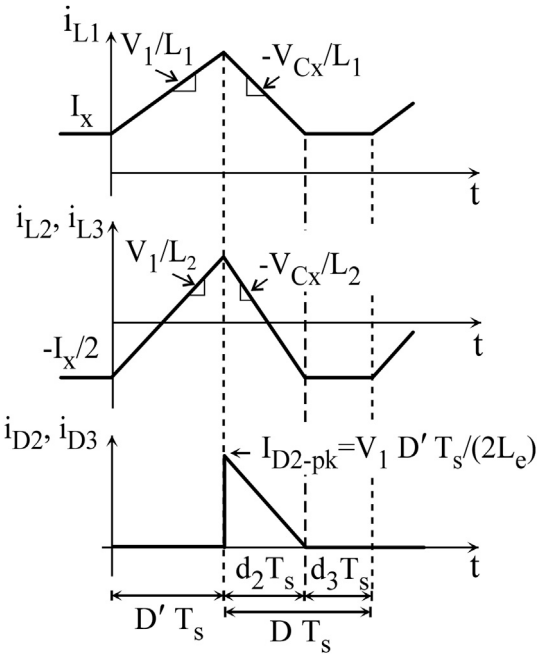

Fig. 8. Inductor current waveforms in DCM for boost mode ($L_2 = L_3$).

Table 1
Normalized component voltage and current stresses for the converter of Fig. 4(a).

Switch Q_1 rms current	$\sqrt{M(2+M)}$
Switch Q_2 and Q_3 rms current	$\sqrt{1+\frac{M}{2}}$
Capacitor C rms current	$\sqrt{2M}$
Capacitor C_x and C_y rms current	$\sqrt{\frac{M}{2}}$
Inductor L_2 and L_3 average current	1
Switch Q_1, Q_2, and Q_3 peak voltage	½+1/M
Capacitor C peak voltage	1/M
Capacitor C_x and C_y peak voltage	½

In addition parasitic resistance (i.e., on-state switch resistance (R_{DS-ON}); capacitor and inductor equivalent series resistance (ESR)) can also be incorporated into the model.

3. The proposed bi-directional converter with coupled inductors

The proposed converter structure utilizes three inductors which are often described as a disadvantage. However, the three inductors have identical voltage waveforms as illustrated in Fig. 6. Hence, they can be magnetically coupled into a single magnetic core as shown in Fig. 10. Accordingly, the converter size, weight, and cost are reduced. In addition, the 'zero-ripple-current' condition at both the input and output terminal can be reached without compromising the converter's performance. This condition is desirable, because the generated EMI noise is minimized, dramatically reducing filtering requirements at both charging and discharging ports. Moreover, the circuit of Fig. 10 can supply free ripple currents in the input and output inductor not only in CCM but also in Discontinuous Conduction Mode (DCM), where the high switching current ripple is of concern. However, DCM mode is not an issue when the switches are synchronously controlled.

Referring to Fig. 10, the input inductor L_1 and the output inductor L_3 are both coupled to L_2, and L_1 and L_3 are not directly coupled. Moreover, by proper selection of the coupling coefficients, k_{12} and k_{23}, near zero current ripples in the inductors at both ends of the bidirectional converter can be obtained. In reality, the ripple current is not exactly reduced to zero, but it is highly reduced. The

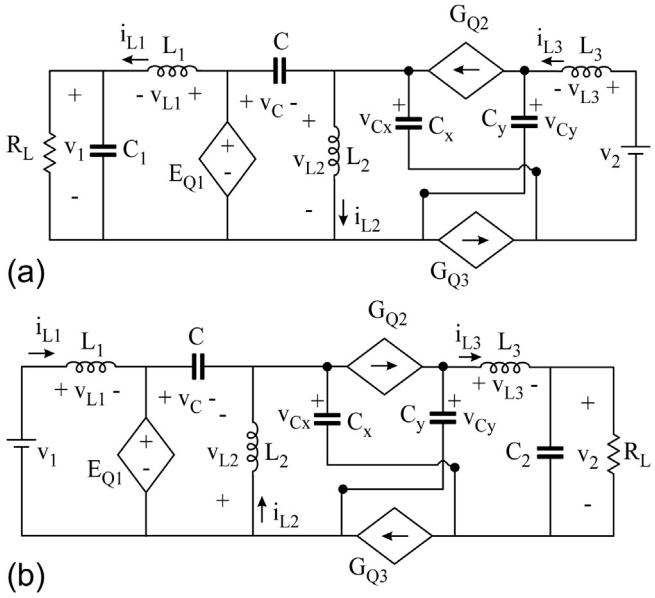

Fig. 9. Averaged circuit model for the converter of Fig. 4(a) in CCM. (a) Buck mode. (b) Boost mode.

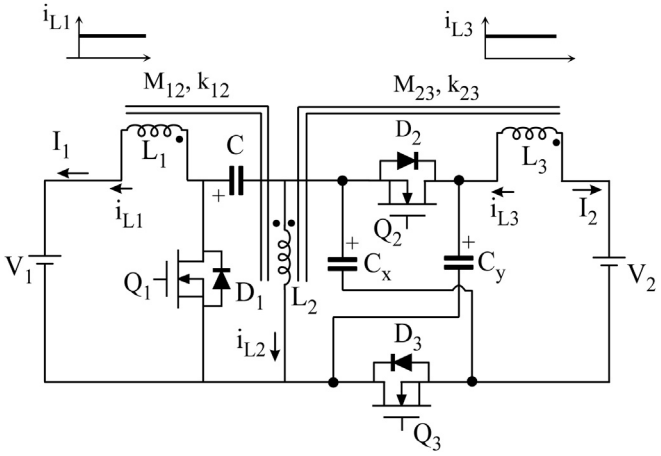

Fig. 10. The proposed converter with coupled inductors.

reason for this is that the voltages across the inductors are not exactly identical due to the ripple voltage across the capacitors.

From Fig. 10, the rate of change of the inductor currents i_{L1}, i_{L2}, and i_{L3} during switch Q_2 and Q_3 off-time is given by,

$$\frac{d}{dt}\begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \end{bmatrix} = \frac{1}{\Delta}\begin{bmatrix} L_2L_3 - M_{23}^2 & M_{12}(M_{23}-L_3) & M_{12}M_{23} \\ -M_{12}L_3 & L_1(L_3-M_{23}) & -M_{23}L_1 \\ M_{12}M_{23} & L_1(L_2-M_{23}) - M_{12}^2 & L_1L_2 - M_{12}^2 \end{bmatrix} \times \begin{bmatrix} V_1 \\ V_C \\ 2V_{CX} - V_2 \end{bmatrix} \tag{23}$$

where

$$\Delta = L_1L_2L_3 - L_1M_{23}^2 - L_3M_{12}^2 > 0 \tag{24}$$

and

$$M_{12} = k_{12}\sqrt{L_1L_2},\ M_{23} = k_{23}\sqrt{L_2L_3} \tag{25}$$

are the mutual inductances of the windings. At steady state, $V_C = V_1$ and $V_2 = 2\,V_{Cx}$, then from [19] the following two conditions must be satisfied for zero ripple in the input and output inductors,

$$\frac{di_{L1}}{dt} = \frac{V_1}{\Delta}\left[L_2L_3 + M_{12}(M_{23}-L_3) - M_{23}^2\right] = 0 \tag{26}$$

$$\frac{di_{L3}}{dt} = \frac{V_1}{\Delta}\left[L_1L_2 + M_{23}(M_{12}-L_1) - M_{12}^2\right] = 0 \tag{27}$$

respectively. In other words, the ripple at the input and output inductors are steered toward L_2. Solving [25] and [26] provides the conditions for zero input/output current ripples as follows,

$$M_{12} = M_{23} = L_2 \Rightarrow \begin{cases} k_{12} = \sqrt{\frac{L_2}{L_1}} & , L_2 < L_1 \\ k_{23} = \sqrt{\frac{L_2}{L_3}} & , L_2 < L_3 \end{cases} \tag{28}$$

with

$$(k_{12})^2 + (k_{23})^2 < 1 \tag{29}$$

During switch Q_2 and Q_3 on-time, the conditions for zero ripple in the input and output inductors are similar to that of [27]. It is important to mention here that the voltage gain for the proposed converter is independent of the magnetic coupling coefficient k. In

other words, the DC voltage gain in [6] and [12] are valid whether using three separate inductors (three cores) or three coupled inductors (single core). It should be also mentioned here that the zero ripple input and output current feature for the converter of Fig. 10 can also be obtained in the conventional Cuk converter using coupled inductors [41]. However, the proposed converter has an advantage of a wider voltage conversion ratio, reduced switch and diode voltage stresses, better switch utilization, and non-inverted output polarity.

The steady-state analysis presented in Section II for the uncoupled inductors is also valid for the coupled-inductor extension, except for the definition of the effective inductance L_e [16]. This is because only inductor L_2 determines the switching current ripple. Thus, for the coupled-inductor case, the definition of L_e becomes $L_e = L_2$. Thus, the minimum required value for L_2 which ensure CCM operation can be found from [18] and [20] and it is given by

$$L_2 > \frac{D^2 R_{L-max} T_s}{8} \tag{30}$$

Once the value of L_2 is chosen the values of L_1 and L_3 can be calculated from [28]. Assuming the inductors L_1 and L_3 have equal values, then from [28] we get

$$L_1 = L_3 > 2L_2 \tag{31}$$

Selection of the capacitors is generally selected to limit voltage ripple to the level required by the specification. The filter capacitors C_1 and C_2 only filter the ac component of the inductors current of L_1 and L_3, respectively. Therefore, the peak to peak voltage ripple across C_1 and C_2 can be calculated from,

$$\Delta v_1 = \frac{\Delta i_{L1} T_s}{8C_1} = \frac{DT_s^2 V_1}{16 L_1 C_1 M_C} \tag{32}$$

$$\Delta v_2 = \frac{\Delta i_{L3} T_s}{8C_2} = \frac{DT_s^2 V_2}{16 L_3 C_2} \tag{33}$$

respectively. Referring to Fig. 6, the peak to peak voltage ripple across capacitors C and C_x (or C_y) can be determined as

$$\Delta v_C = \frac{I_{L1} D T_s}{C} = \frac{DT_s P_{in}}{C V_1} \tag{34}$$

$$\Delta v_{Cx} = \Delta v_{Cy} = \frac{I_{L1} D T_s}{2C_x} = \frac{DT_s P_{in}}{2C_x V_1} \tag{35}$$

respectively. Also, selection of capacitors C and C_x must ensure that the converter does not operate discontinuous capacitor voltage mode (DCVM). Therefore, the resonant frequencies of (L_2, C) and (L_2, $2C_x$) should be lower than the switching frequency f_s to assure the capacitor voltages V_C and V_{Cx} to be constant in a switching period.

4. Simulation and experimental results

Circuit simulation and experimental tests were conducted for the proposed converter of Fig. 4(a) in the charging and discharging power direction to validate the theoretical results and to measure its performance in terms of efficiency. The converter operation is verified at the following operating point: $V_2 = 180$ V, battery voltage $V_1 = 24$ V, and output power $P_o = 100$ W at switching frequency $f_s = 66$ kHz. The inductors' and capacitors' values are set to 680 μH and 47 μF, respectively.

4.1. Simulation verification

Pspice actual semiconductor models have been used to simulate the active switches. The IXFT50N20 MOSFET is used for Q_1, Q_2 and Q_3. An equivalent series resistance (ESR) of 50 mΩ is connected in series with each capacitor and inductor to model its losses.

Fig. 11 shows the simulated waveforms for the converter of Fig. 4(a) in the charging mode ($V_2 = 180$ V → $V_1 = 24$ V). In the presented simulated results, the switches are not controlled in a synchronized manner; the body diode of the non-active switch Q_1 was biased passively. It should be noted that operating the switches in charging or discharging modes as synchronous switches, minimizes the drawback of the reverse recovery current of the MOSFET body diode and guarantees that the controller is always operating in CCM. Fig. 11(a) shows the current ripple at the input and output ports. Note that the ripple current flowing through the two inductors L_1 and L_3 are almost equal in magnitude which confirms that their voltages are equal. Fig. 11(b) presents the simulated voltage and current waveforms of the body diode of Q_1. The voltage/current waveforms of switch Q_2 are shown in Fig. 11(c). Voltage and current waveforms of switch Q_3 are the same as Q_2. It is evident from Fig. 11(b) and (c) that the voltage stresses across the power switches are smaller than the high-side voltage V_2.

Fig. 12 shows the simulated waveforms for the converter of Fig. 4(a) in the discharging mode ($V_1 = 24$ V → $V_2 = 180$ V). In this

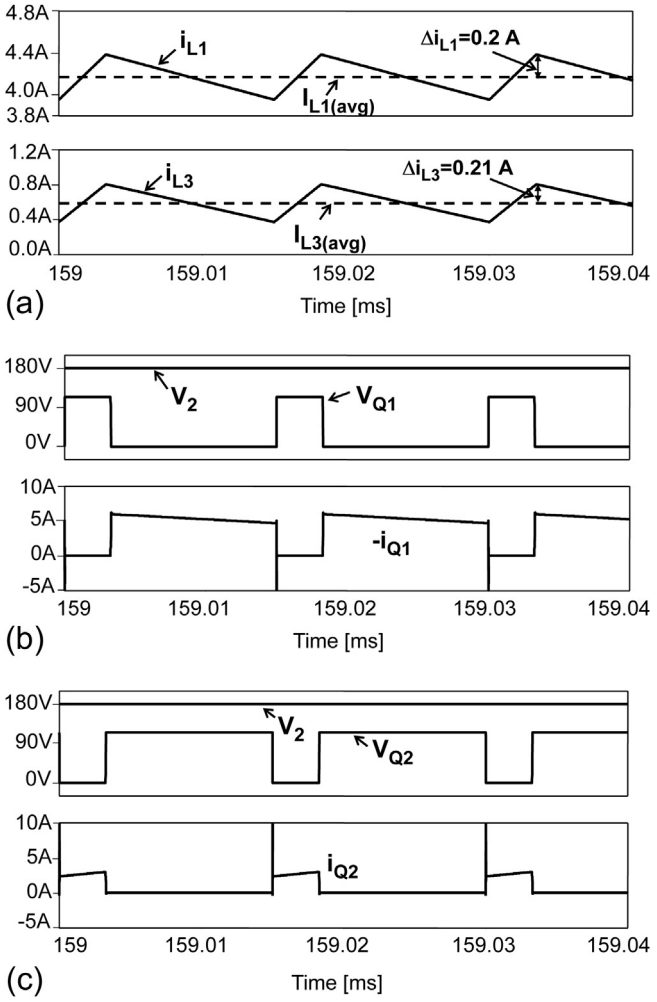

Fig. 11. Simulated waveforms for the converter of Fig. 4(a) in CCM with three separate inductors. (Charging mode).

case, only the power switch Q_1 is controlled while the body diodes of the non-active switches Q_2 and Q_3 were biased passively. Similar to the results obtained in the charging mode, Fig. 12(a) shows the current ripple at the input and output ports with equal ripple current flowing through L_1 and L_3 which confirms that their voltages are equal. Fig. 12(b) presents the simulated voltage and current waveforms of the active power switch Q_1. The voltage/current waveforms of the body diode of switch Q_2 are shown in Fig. 12(c). The simulated waveforms suggest a good agreement with theory whether the converter is operating in buck charge mode or boost discharge mode.

In order to demonstrate the effect of coupling the inductors on the converter input and output current ripples, the circuit of Fig. 10 has been simulated with coupled inductors. The circuit parameters were all the same as those for the uncoupled case except for the value of L_2 which is set to 330 μH. Thus, the values of both coupling coefficients k_{12} and k_{23} are set to 0.7. The simulated input and output inductors current (i_{L1} and i_{L3}) waveforms are shown in Fig. 13. It is evident from Fig. 13 that the high frequency switching ripples' magnitude in the i_{L1} and i_{L3} is greatly reduced due to the coupling of the three inductors. Thus, the generated EMI noise level is greatly minimized as well as the requirement for the input filtering. Another advantage of coupling the three inductors is a significant reduction in total rms input and output current, which in turn allows less expensive capacitors to be used at the input/output port of the converter.

The performance of the converter of Fig. 4(a) is further investigated under conditions of load current and input voltage changes

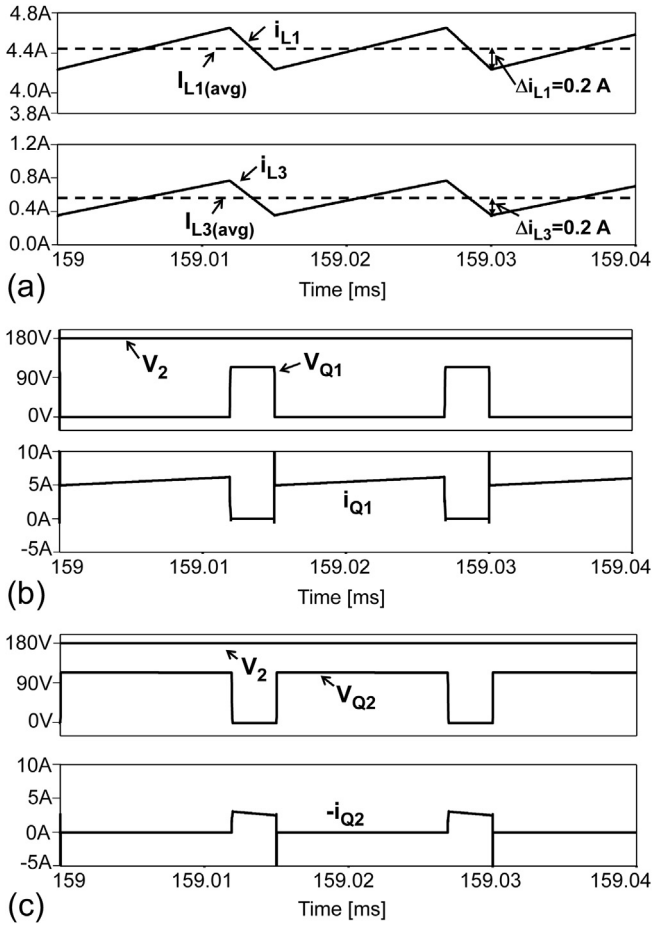

Fig. 12. Simulated waveforms for the converter of Fig. 4(a) in CCM with three separate inductors. (Discharging mode).

based on the average circuit model of Fig 9. The converter state equations can be obtained directly from the average circuit model. For example, referring to Fig. 9(a), the six state variables can be derived as:

$$L_1\frac{di_{L1}}{dt} = d(v_C + v_{Cx}) - v_1 \qquad C\frac{dv_C}{dt} = d'(i_{L2} + i_{L3}) - di_{L1}$$
$$L_2\frac{di_{L2}}{dt} = dv_{Cx} - d'v_C \qquad C_x\frac{dv_{Cx}}{dt} = \frac{(1+d')}{2}i_{L3} - \frac{d}{2}(i_{L1} + i_{L2})$$
$$L_3\frac{di_{L3}}{dt} = v_2 - d'v_C - (1+d')v_{Cx} \qquad C_1\frac{dv_{C1}}{dt} = i_{L1} - \frac{v_1}{R_L} \tag{36}$$

where d represent switch Q_2 and Q_3 duty-cycle and $d' = 1 - d$. Note that the two capacitors C_x and C_y is represented by a single state variable since the voltage across both of them has to be the same. The small-signal ac equations are obtained by perturbation and linearization of [35], where the variables are decomposed in the DC (X) component and the small ac variations ($\hat{x}$) component and then eliminating the 2nd order terms, we can write the linearized small-signal converter equations as:

$$\frac{d}{dt}\begin{bmatrix}\hat{i}_{L1}\\ \hat{i}_{L2}\\ \hat{i}_{L3}\\ \hat{v}_C\\ \hat{v}_{Cx}\\ \hat{v}_1\end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{D}{L_1} & \frac{D}{L_1} & \frac{-1}{L_1}\\ 0 & 0 & 0 & \frac{-D'}{L_2} & \frac{D}{L_2} & 0\\ 0 & 0 & 0 & \frac{-D'}{L_3} & \frac{-(1+D')}{L_3} & 0\\ \frac{-D}{C} & \frac{D'}{C} & \frac{D'}{C} & 0 & 0 & 0\\ \frac{-D}{2C_x} & \frac{-D}{2C_x} & \frac{(1+D')}{2C_x} & 0 & 0 & 0\\ \frac{1}{C_1} & 0 & 0 & 0 & 0 & \frac{-1}{R_LC_1}\end{bmatrix}\begin{bmatrix}\hat{i}_{L1}\\ \hat{i}_{L2}\\ \hat{i}_{L3}\\ \hat{v}_C\\ \hat{v}_{Cx}\\ \hat{v}_1\end{bmatrix} + \begin{bmatrix}\frac{1}{L_1}\frac{V_1}{D} & 0\\ \frac{1}{L_2}\frac{V_1}{D} & 0\\ \frac{1}{L_3}\frac{V_1}{D} & \frac{1}{L_3}\\ \frac{-1}{C}\frac{V_1}{R_LD'} & 0\\ \frac{-1}{C_x}\frac{V_1}{R_LD'} & 0\\ 0 & 0\end{bmatrix}\begin{bmatrix}\hat{d}\\ \hat{v}_2\end{bmatrix} \tag{37}$$

Note that, the quiescent values D, D′, and V_1, are treated as given constants in the equations. Due to the complexity of the system with the six equations, the desired transfer function can be obtained using any generic computational software. The simulated frequency response of the open-loop small-signal transfer functions of input voltage (v_2)-to-output voltage (v_1) and control-to-output voltage (v_1) are shown in Fig. 14(a) and (b), respectively. The parameters used to generate the bode plot are as follows:

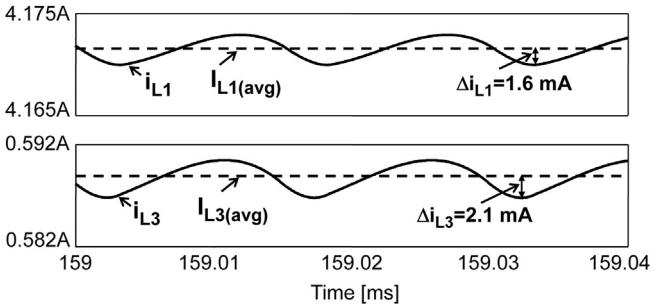

Fig. 13. Simulated waveforms for the converter of Fig. 10 with coupled inductors.

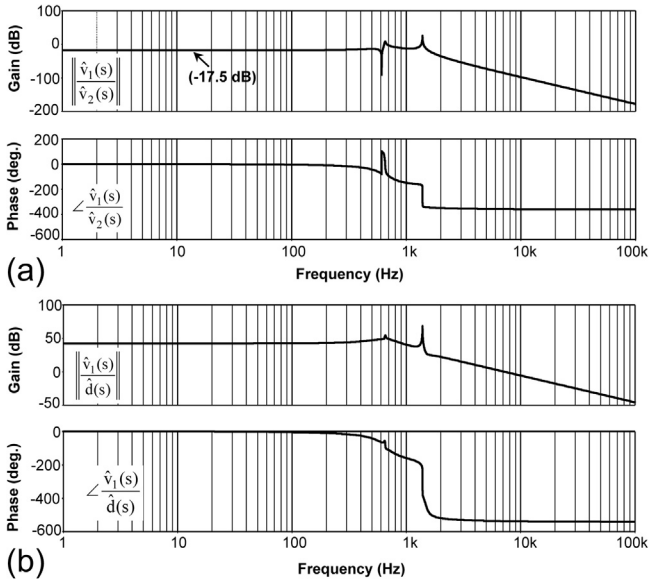

Fig. 14. Open loop frequency responses (charging mode). (a) Input voltage-to-output voltage. (b) Control-to-output voltage.

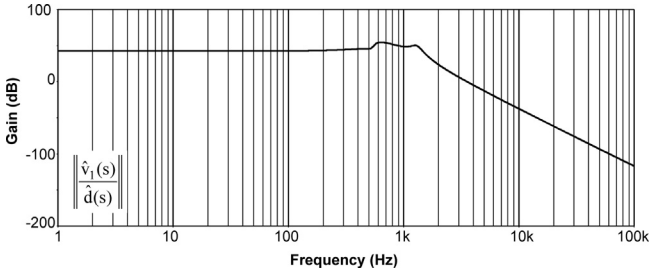

Fig. 15. Control-to-output voltage frequency response (charging mode) with damping circuit ($R_d = 10\ \Omega$, $C_d = 20\ \mu F$).

$V_2 = 180$ V, $L_1 = L_2 = L_3 = 680\ \mu H$, $C = C_x = C_y = 47\ \mu F$, $C_1 = 80\ \mu F$, $R_L = 5.76\ \Omega$, and $D = 0.21$.

Note that Fig. 14(a) predicts correctly the expected dc voltage gain of (−17.5 dB) which is equivalent to ($V_1/V_2 = 24/180$). Also, as shown in Fig. 14, there are 2 resonance locations with high Q-factor. This will cause oscillations which makes the system unstable. Designing a controller that lacks a damping circuit to prevent resonance with high Q goes beyond the scope of this paper. An easy solution to reduce the Q-factor and to prevent from oscillation is to implement $R_d - C_d$ damping circuit parallel with the three capacitors (C, C_x, and C_y). Fig. 15 shows a small-signal response of control-to-output voltage. As shown in Fig. 15, there is a great reduction in the resonant Q-factor due to the damping circuit. It could make a different magnitude of resonance depend on selections of $R_d - C_d$ parameters by simulation. The total power loss in the damping circuit could be ignored because it is only under 1 − W.

Based on the open-loop transfer function of the system, a classical type-III compensation network is designed. The simulated transient response of the output voltage in response to a step

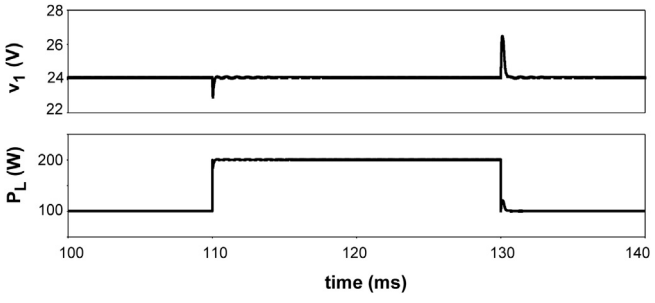

Fig. 16. Simulated closed-loop transient response of the output voltage (top trace) and load power (lower trace) when subjected to an output load change from 100 W to 200 W−100 W (Charging mode).

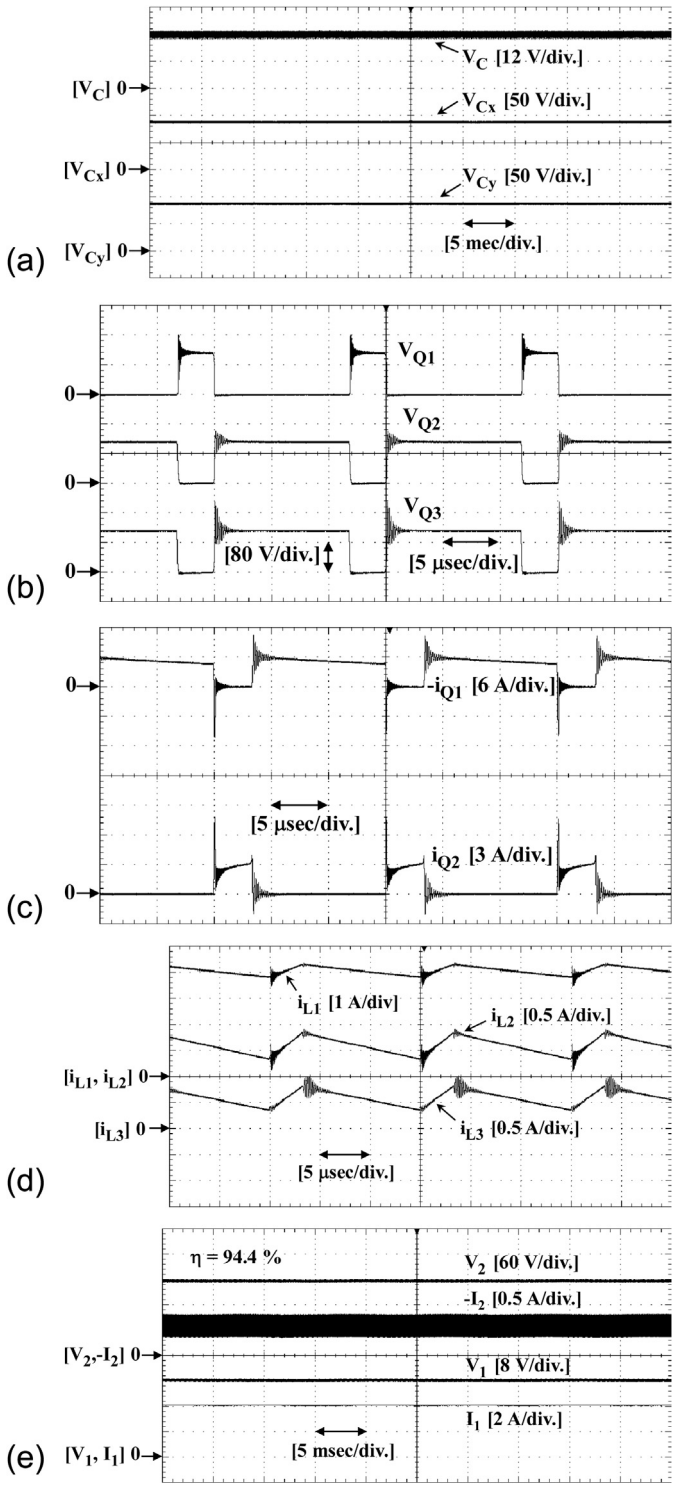

Fig. 17. Measured waveforms for the converter of Fig. 4(a) in the charging mode ($V_2 = 180$ V → $V_1 = 24$ V).

changes in load current is shown in Fig. 16. It can be observed from Fig. 16 that the recovery time is less than 5 ms.

4.2. Experimental results

A 100-W prototype of the proposed converter of Fig. 4(a) has been built to validate the theoretical prediction as well as the simulation previously described. The circuit parameters of the experimental setup are the same as those used for simulation. The converter performance was verified in the charging mode (V_2 = 180 V → V_1 = 24 V) and discharging mode (V_1 = 24 V → V_2 = 180 V) power flow.

The key waveforms of the experimental prototype in the charging power flow mode at full-load power are depicted in Fig. 17. In this case, switch Q_1 is held off and the load voltage V_1 is regulated by control of the duty-cycle of Q_2 and Q_3. According to [6], the

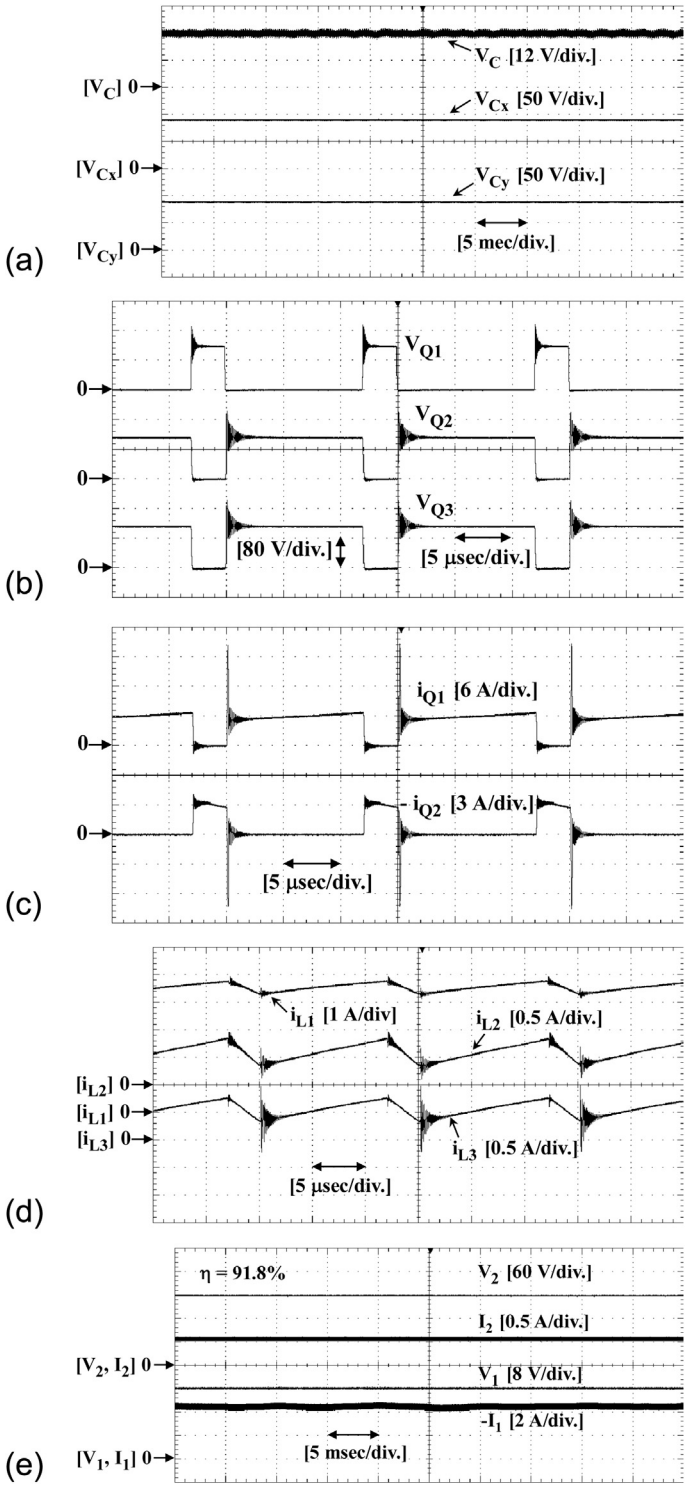

Fig. 18. Measured waveforms for the converter of Fig. 4(a) in the discharging mode (V_1 = 24 V → V_2 = 180 V).

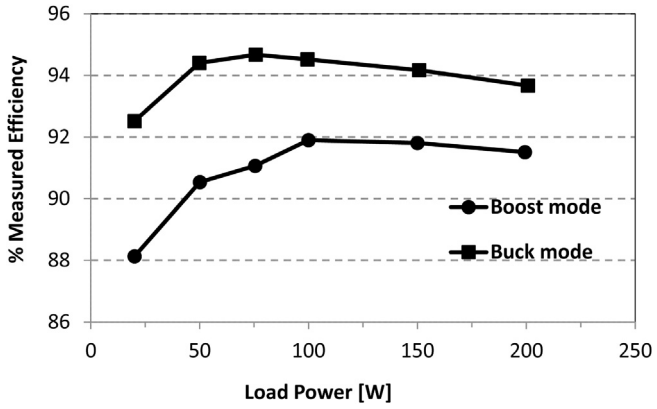

Fig. 19. Measured efficiency for the converter of Fig. 4(a) in the charging mode (Buck mode) and discharging mode (boost mode).

switch duty-cycle is equal to 0.21. The voltage waveforms across capacitors C, C_x, and C_y are shown in Fig. 17(a). Note that the voltage across capacitor C is equal to the load voltage V_1. Fig. 17(b) shows the voltage waveforms across the three switches (Q_1, Q_2, and Q_3). Referring to Fig. 17(b), it is clear that the maximum voltage across the switches is clamped slightly above the normalized voltage of $(1/2 + M_C)$ as expected. Fig. 17(c) illustrates the switching current waveforms through Q_1 and Q_2. Switch Q_3 current waveform is not shown since it is similar to the switch Q_2 current waveform. Referring to Fig. 17(c), the current through Q_1 actually represents the current flowing through its intrinsic body diode (D_1) because the switch Q_1 is not actively switched on in the charging mode. Notice that the current spike at the turn-off of MOSFET Q_1 is mainly due to the MOSFET body diode, which is typically a slow "un-optimized" diode. The waveforms of the three inductors' currents are depicted in Fig. 17(d) for several switching periods which clearly demonstrate CCM operation. Note that the measured inductors' current ripples show very close agreement with the simulation results. Fig. 17(e) shows input/output voltage and current waveforms which verifies that [6] is satisfied. Based on the measured input/output current and voltage waveforms shown in Fig. 17(e), the efficiency in the charging power flow direction is about 94.4%.

Similarly, Fig. 18 shows measured waveforms at full-load power of the same prototype in the discharging mode ($V_1 = 24$ V → $V_2 = 180$ V). In this case, only switch Q_1 is controlled by pulse width modulator (PWM) while the other switches Q_2 and Q_3 are held off. According to (12), the switch Q_1 duty-cycle is set close to 0.78. Fig. 18(a) shows the steady-state voltage waveforms across capacitors C, C_x, and C_y. Referring to Fig. 18(a), it is clear that the voltage across capacitor C is equal to the input voltage V_1 while the voltages across capacitors C_x and C_y are very close to the theoretical predicted value given in [10]. Fig. 18(b) shows the voltage waveforms across the three switches (Q_1, Q_2, and Q_3).

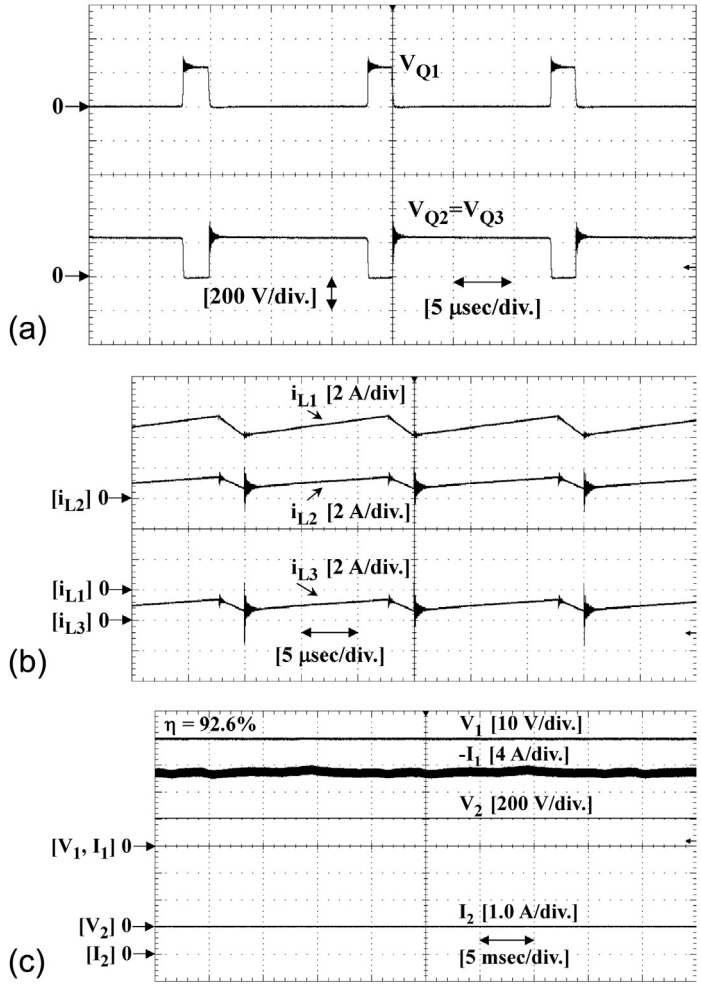

Fig. 20. Measured waveforms for the converter of Fig. 4(a) in the discharging mode ($V_1 = 40$ V → $V_2 = 400$ V).

Referring to Fig. 18(b), it is apparent that the switches in the discharge mode are subjected to similar voltage stress as in the case of charging mode. Fig. 18(c) shows the switching current waveforms through Q_1 and Q_2. Note that the current through Q_2 actually represents the current flowing through its intrinsic body diode (D_2) because the switch Q_2 is not actively switched on in the discharging mode. The waveforms of the three inductors' currents are depicted in Fig. 18(d) for several switching periods which clearly demonstrate CCM operation with current ripples close to the predicted theoretical values. Finally, Fig. 18(e) shows input/output voltage and current waveforms which verifies that [12] is satisfied. Based on the measured input/output current and voltage waveforms shown in Fig. 18(e), the efficiency in the discharging power flow direction is about 91.8%. The difference in charging and discharging efficiencies is mainly due to the high losses of the body diodes of the MOSFETs which typically are slow resulting in high reverse recovery current, hence, lower efficiency. The MOSFET is typically optimized around its switching capability and not the performance of the body diode. In the discharging mode there are two body diodes conducting (D_2 and D_3) during part of the switching cycle while it is only one diode (D_1) in the charging mode.

Fig. 19 depicts the measured efficiencies of the experimental prototype for both charging and discharging mode as a function of the load power. The efficiency curves are obtained in the absence of any snubber circuits across the switches. As can be seen from Fig. 19, the efficiency curve for the charging mode is higher than the discharging mode case. This is because in the discharging mode two body diodes (D_2 and D_3) will conduct while in the charging mode only the body diode (D_1) of Q_1 conducts. These MOSFET body diodes have a high forward drop compared to the $R_{ds(ON)}$ of the MOSFET, which translates to $(V_F \times I) >> (I_{rms} \times R_{ds(ON)})$; hence, higher losses. One way to mitigate this issue is to run the MOSFET in a synchronous manner. Nevertheless, the converter can achieve more than 91% conversion efficiency under nominal operation conditions.

The proposed converter of Fig. 4(a) has been also tested for different input and output voltage levels. Fig. 20 shows the key waveforms at the experimental prototype at 400-W in the discharging mode ($V_1 = 40\,V \rightarrow V_2 = 400\,V$). The circuit parameters of this experimental setup are: $L_1 = 360\,\mu H$, $L_2 = L_3 = 680\,\mu H$, $C = 30\,\mu F$ (polypropylene film capacitor), $C_x = C_y = 20\,\mu F$ (Polypropylene film capacitor), $C_2 = 80\,\mu F$ (electrolytic type), and STY60NM50 (500 V, 60 A, 45 mΩ) for the active switches. The converter is switched at 66 kHz and according to [12], the switch Q_1 duty-cycle is set close to 0.833. Fig. 20(a) shows switch Q_1 and Q_2 blocking voltage waveforms. Switch Q_3 waveform is not shown since it is similar to the switch Q_2 waveform. It is evident from Fig. 20(a) that the switch voltage stress is close to the theoretical predicted value (240 V) as given in Table 1. The waveforms of the three inductors' currents are depicted in Fig. 20(b). The measured inductors' current ripples appear to be in very good agreement with theoretical design values. The input/output voltage and current waveforms are depicted in Fig. 20(c) which verifies that [12] is satisfied. The circuit efficiency at 400-W is about 92.6%.

It is important to mention here that the experimental prototype has been conceived on a proof-of-concept basis; therefore, the components have been chosen based on their off-the-shelf availability rather than optimizing the performance of the converter. Therefore, the reported measured efficiencies can be improved further by improving the layout and utilizing better components.

5. Conclusion

High-gain and zero-current ripple topology has been presented for high-efficiency fuel cell powertrain applications. Bidirectional converters have gained wider interest with the rise of renewable energy applications. The proposed converter topology has a wide voltage conversion range and low switch voltage stress. Measurements confirm a high efficiency capability of the proposed converter in the charging mode of 94.4%. The proposed topology requires a single control signal which makes its control fairly simpler compared to other low ripple DC–DC or bi-directional topologies. The coupled magnetic characteristics improve the power density of the converter and result in an almost near zero input/output current ripple. The low ripple current results in an improved durability for the fuel cell. Moreover, the high voltage gain capability coupled with the low current ripple at the battery side allows the utilization of less expensive low voltage energy storage batteries with a longer life span; hence, a higher quality system. The performance of the proposed converter has been verified by simulation and detailed experimental results in both charging and discharging modes.

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